[21] 20. An IPSec cryptography acceleration chip, comprising:

an external system bus interface unit;

a packet classifier unit:

a packet distributor unit;

a FIFO input buffer connected to the packet classifier unit;

a FIFO output buffer connected to packet distributor unit;

a plurality of cryptography processing engine units connected to the packet distributor unit; and

a control processor that manages the processing of packets through the chip.

[22] 21. The IPSec cryptography acceleration chip of Claim [21] 20, further comprising:

a packet splitting unit, in which incoming packets are split into fixed-sized cells.

[23] 22. A network communication device, comprising:

a central processing unit;

a system memory;

a network interface unit;

a cryptography acceleration chip comprising:

a plurality of cryptography processing engines; and